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(54) Title: POWER MOSFET

(57) Abstract: A system of interconnecting regions on an integrated semiconductor device or discrete components. As first connectivity layer has first and second runners to interconnect a plurality of first and second regions. A second connectivity layer has third runners to interconnect the first runners and fourth runners to interconnect the second runners. A third connectivity layer has first pads connected to the third runners and second pads connected to the fourth runners. Solder bumps are used on the first and second pads to connect the pads to other circuits.

TITLE

[0001] POWER MOSFET

CROSS-REFERENCE TO RELATED APPLICATIONS.

[0002] This application claims the benefit of United States Patent Application 10/601,121 filed June 19, 2003 and United States Provisional Application 60/416,942 filed October 8, 2002, each of which are hereby incorporated by reference in its entirety.

BACKGROUND OF THE INVENTION

1. Field Of The Invention

[0003] The present invention generally relates to the field of semiconductor devices and methods of interconnecting them.

2. Related Background Art

[0004] Conventional lateral power metal-oxide semiconductor field effect transistors ("MOSFETs") are currently available. However, these conventional lateral power MOSFETs exhibit problems of high on-state resistance due to the parasitic resistance of metal interconnects. This is typically caused by long and thin interconnects that are used in connecting the transistor cells and in connecting the external leads of the devices. This problem is exacerbated when the die size of the transistor is scaled up and a large number of transistor cells are connected in parallel to handle greater power loads.

[0005] Conventional lateral power MOSFETs are also formed using complementary metal-oxide semiconductor ("CMOS") processes. A conventional process may require 18 masks for a 3 metal layer process. The complexity of such a process increases the fabrication costs, errors, and also problems with latch-up.

[0006] Bipolar devices are also susceptible to the same problems as MOSFETs with high on-state resistance due to the parasitic resistance of the metal interconnects for similar reasons.

[0007] Accordingly, there is a need to provide lateral power devices, such as MOSFETs and biplolar devices, with reduced parasitic resistance of interconnects to reduce on-state resistance. In the case of MOSFETs, there is also a need for fabricating lateral power MOSFETs using fewer processing steps than conventionally used.

BRIEF SUMMARY OF THE INVENTION

[0008] The present invention discloses a system for interconnecting regions on a semiconductor substrate using wide metal runners or a planar interconnection layer, and a plurality of solder bumps on conductive pads arranged in a checkerboard pattern or interleaved, thereby reducing parasitic resistance. The interconnections may be used for connecting discrete as well as integrated devices.

BRIEF DESCRIPTION OF THE DRAWINGS

[0009] Figures 1-6 below depict various aspects and features of the present invention in accordance with the teachings herein.

[0010] It will be appreciated that for simplicity and clarity of illustration, elements illustrated in the figures have not necessarily been drawn to scale. For example, the dimensions of some of the elements are exaggerated relative to other elements for clarity. Further, where considered appropriate, reference numerals have been repeated among the figures to indicate corresponding or analogous elements.

DESCRIPTION OF THE INVENTION

[0011] The preferred embodiment of the present invention uses conventional CMOS fabrication processes to fabricate a semiconductor device embodying the present invention to reduce the costs of production. In accordance with one aspect of the present invention, however, only one type of MOSFETs (either an n-channel or p-channel MOSFET) is made on the die. Since the device of the present invention only consists of parallel n-channel or p-channel transistors, the problem of latch-up is avoided.

[0012] In another preferred embodiment no field implants are used, although alternate embodiments may use field implants if there is more than one transistor on a die.

[0013] Yet further, in another preferred embodiment of the invention there is no local field oxide layer since the preferred embodiment is constructed having only one device per die.

[0014] Yet further, in another preferred embodiment of the invention a self-aligned sicilide is formed over the source, drain and gate of the transistor.

[0015] One advantage to using the simplified process flows is that in the preferred embodiment, the process masks are reduced from 18 masks for a 3 metal layer process to 10 masks.

[0016] In a preferred embodiment of the present invention the transistor cells are interconnected by runners that are short and wide in comparison to prior art devices. The

[0017] FIG. 1a shows one embodiment of the present invention in perspective view. In particular, there is shown a portion of a semiconductor device 100 having two sources 110 and a drain 120. In the illustrative example, device 100 is shown with a P substrate

105. In another embodiment, P substrate 105 is deposited on top of a P- substrate (not shown).

[0018] Sources 110 and drain 120 are preferably n-type dopant implants into P substrate 105. It will be appreciated that variations of the design of the sources and drains are known to one skilled in the art and within the scope of the present invention. For example, sources 110 and drain 120 could be p-type dopant implants into an N substrate 105.

[0019] As another example, FIG 1b shows a preferred embodiment where sources 110B is comprised of a region 112 which is doped as N+, region 114 which is doped as P+ and region 116 which is doped an N. In an alternate embodiment, source 110B is comprised of region 114 doped as P+, and regions 112 and 116 are N+ implants adjacent to either side of the P+ region 114. In yet another embodiment, regions 112 and 114 also have a region 118. Region 118 may be a lightly doped N- implant while the rest of regions 112 and 114 are N+. Region 118's lightly doped N- implant functions as a lightly doped drain.

[0020] In FIG. 1b, drain 120B, in this example, is comprised of region 124 doped as N+ and regions 124 and 126 doped as N. As with the source 110B, it is within the scope of the invention and the skill of one skilled in the art to vary the doping.

[0021] Referring back to the embodiment shown in FIG. 1a, gate 130 is comprised of a polysilicon gate over a SiO_2 or Si_3N_4 insulating layer (not shown) and is placed between source 110 and drain 120. Adjacent to gate 130 are spacers 132 and 134, preferably comprised of SiO_2 or Si_3N_4, and partially extending over source 110 and drain

120, respectively. (FIG. 1b also shows spacers 132 and 134 extending over regions 118 and 122. Spacers also extend over region 126.)

[0022] Source runners 140 and drain runners 150 are formed on a first interconnect layer and is preferably comprised of metal, although other conductive materials may be used. In particular, multiple sources 110 are interconnected by source runner 140 using vias 142. Preferably source runner 140 is in a substantially orthogonal orientation to source 110 and drain 120, although other orientations that are not orthogonal (for instance, angled or even parallel) may be used.

[0023] Drains 120 are interconnected by drain runners 150 using vias 152. Preferably, drain runner 150 is in a substantially orthogonal orientation to drain 120, although other orientations that are not orthogonal (for instance, angled or even parallel) may be used.

[0024] For the sake of clarity, FIG. 1a shows only one drain 20, but in the preferred embodiment there multiple drains 120 would be interleaved between multiple sources 110. Likewise, only one source runner 140 and drain runner 50 are shown, but in the preferred embodiment there are multiple source and drain runners 140 and 150 and are, preferably, interleaved with each other.

[0025] FIG. 1a also shows source runners 160 and drain runners 170 formed on a second interconnect layer and is preferably comprised of metal, although other conductive materials may be used. Source runner 160 interconnects source runners 140 using vias 162. Preferably source runners 160 are in a substantially parallel orientation with respect to source 110, although other orientations that are not parallel (for instance, angled) may be used.

[0026] Drain runners 150 are interconnected by drain runners 170 using vias 172. Preferably, drain runner 170 is in a substantially parallel orientation with respect to drain 120, although other orientations that are not parallel (for instance, angled) may be used.

[0027] Like the first interconnect layer, only one source and drain runners 160 and 170, respectively, are shown, but in the preferred embodiment multiple source and drain runners 160 and 170 would be used and are, preferably, interleaved with each other.

[0028] Although the runners shown in FIG. 1a are substantially of equal widths and rectangular, the runners can be of any shape. For instance, runners may be of unequal widths and runners may have varying narrow and wider portions or rounded corners.

[0029] FIG. 1a shows source pad 180 formed on a third interconnect layer, which is preferably comprised of metal, although other conductive materials may be used. Source pad 180 is connected to source runners 160 using vias 182. Also shown is solder bump 184 formed on source pad 180. Although not shown in FIG. 1a for the sake of clarity, similar drain pads (see FIG. 1c, drain pad 190 as an example) and solder bumps connect drain runners 170 via solder bumps and likewise for gate pads and solder bumps. These solder bumps provide connections between the sources 110, drains 120, and gates 130 with external circuits.

[0030] In the preferred embodiment the vias (for instance vias 142, 152, 162, 172 and 182) form conductive interconnects and are comprised preferably out of tungsten, although other conductive material may be used. These are formed in a manner that are well-known to those skilled in the art.

[0031] In another embodiment, no second interconnect layer is used for runners. As an example, FIG. 1c shows an embodiment similar to FIG. 1a except there is no second

interconnect layer forming source runners 160 and drain runners 170. Instead, drain pad 190 is formed on the second interconnect layer and is connected to drain runners 150 by vias 172. Solder bump 194 is formed on drain pad 190. Although not shown in FIG. 1c for the sake of clarity, similar source pads and solder bumps connect source runners 140.

[0032] Referring now to FIG. 2 there is shown a top plan view of the embodiment shown in FIG. 1a and showing additional sources 110, drains 120 and first layer interconnect source runners 140 and drain runners 150. Sources 110 and drains 120 are shown having a substantially vertical orientation while source runners 140 and drain runners 150 are shown in a substantially horizontal orientation. Also shown are vias 142 and 152 interconnecting the source runners 140 and drain runners 150 to sources 110 and drains 120, respectively. It should be noted that although FIG. 2, for instance, shows at a point of connection the use of two vias, one via could be used, as shown in FIG. 3a, or more than two, as shown in FIG. 1a for vias 182.

[0033] Referring now to FIG. 3a there is shown a top plan view of the embodiment of FIG. 1A showing the first interconnect layer (forming source runners 140 and drain runners 150), second interconnect layer (forming source runners 160 and drain runners 170) and third interconnect layer forming source pad 180 (in outline form).

[0034] Source runners 140 and drain runners 150 are laid out in a substantially horizontal orientation. Source runners 160 overlay source runners 140 and are interconnected using vias 162. Drain runners 170 overlay drain runners 150 and are interconnected using vias 172. Source pad 180 is shown in FIG. 3A overlaying source runners 160 and drain runners 170, but is only connected to source runners 160 by vias 182.

[0035] FIG. 3b shows a top plan view of the embodiment of FIG. 1a showing the first interconnect layer (forming source runners 140 and drain runners 150), second interconnect layer (forming source runners 160 and drain runners 170) and a third interconnect layer forming a drain pad 190 (in outline form).

[0036] Source runners 140 and drain runners 150 are laid out in a substantially horizontal orientation. Source runners 160 overlay source runners 140 and interconnect source runners 140 using vias 162. Drain runners 170 overlay drain runners 150 and interconnect drain runners 170 using vias 172. Drain pad 190 is shown overlaying source runners 160 and drain runners 170, but is only connected to drain runners 170 by vias 192.

[0037] FIG. 4a shows the top of device 100 with source pads 180, analogous drain pads 300 and gate pads 400. Also shown are solder bumps 184 for the source pad, solder bumps 304 for the drain pads, and solder bumps 404 for the gate pads. In the embodiment shown in FIG. 4, the source and drain pads are arranged in a checkerboard layout.

[0038] FIG. 4b shows an alternative layout where each source pad 410 and drain pad 420 are shaped as "stripes" and are interleaved with each other. In the preferred embodiment gate pad 430 would be placed with a shortened source pad 410 or shortened drain pad 420 as needed.

[0039] Another embodiment of the present invention is shown in FIG. 5. In this embodiment sources 520 and drains 530 are laid out in a "checkerboard" pattern. A first interconnect layer forms a source connection layer 500 which interconnects sources 520 using vias 504.

[0040] A second interconnect layer forms a drain connection layer 510 which connects drains 530 though vias 514, through openings in the first interconnect layer and using a cutout portion of that first layer to form connection 502. Drain connection layer 510 then connects to connection 502 using vias 516.

[0041] A third interconnect layer (not shown) would also connect to source connection layer 500 using vias 506, connection 512 and a via connected to connection 512 (not shown). Preferably source connection layer 500, drain connection layer 510 and the third interconnection layer would be comprised of metal or another conductive material and the vias would be comprised of tungsten or other conductive material. This third interconnect layer would be connected to solder bumps in a manner similar to that shown in FIG. 1a.

[0042] FIG. 6a and b show a top plan view. In particular, FIG. 6a shows source connection layer 500 with openings and cutouts 502 to permit connections to drains 530 from drain connection layer 510. FIG. 6b shows drain connection layer 510 for the drains with openings and cutouts 512 to permit access and contact to source connection layer 500, which connects to sources 520.

[0043] It will be appreciated that the present invention is not limited to integrated devices. Using FIG 5 as an example of interconnecting discrete components, if sources 520 and drains 530 were discrete components, those components are interconnected using the present invention in a manner described in more detail above with reference to FIG. 5 as an integrated device. Moreover, it is appreciated that more than two or three interconnect layers may be used and that there may be intermediate interconnect layers

between, for instance, the first and second interconnect layers or between the second and third interconnect layers.

[0044] It should be apparent to those skilled in the art that the foregoing are illustrative only and not limiting, having been presented by way of example only. All the features disclosed in this description may be replaced by alternative features serving the same purpose, and equivalents or similar purpose, unless expressly stated otherwise. Therefore, numerous other embodiments of the modifications thereof are contemplated as falling within the scope of the present invention as defined herein and equivalents thereto.

[0045] What is claimed is:

1. A semiconductor device comprising:

a. a semiconductor substrate;

b. at least one first doped region in said semiconductor substrate forming at least one source;

c. at least one second doped region in said semiconductor substrate forming at least one drain;

d. a first connectivity layer having at least one first runner and at least one second runner, wherein said at least one first runner is operatively connected to said at least one first doped region and said at least one second runner is operatively connected to said at least one second doped region;

e. a second connectively layer operatively connected to said first connectively layer and having at least one third runner and at least one fourth runner, wherein said at least one third runner is operatively connected to said at least one first runner and said at least one fourth runner is operatively connected to said at least one second runner;

f. a third connectively layer having at least one first pad operatively connected to said at least one third runner and at least one second pad operatively connected to said at least one fourth runner.

2. A semiconductor device of claim 1 wherein said at least one first pad has at least one first solder bump and said at least one second pad has at least one second solder bump.

3. A semiconductor device of claim 2 wherein said at least one first pad and said at least one second pad are arranged in a substantially checkerboard pattern.

4. A semiconductor device of claim 2 wherein said at least one first pad is interleaved with said at least one second pad.

5. A semiconductor device of claim 1 wherein said at least one first doped region is a source for a transistor and said at least one second doped region is a drain for a transistor.

6. A semiconductor device of claim 5 wherein said at least one source and at least one drain are laid out in a substantially elongated shape and wherein said at least one source are interleaved with said at least one drain.

7. A semiconductor device of claim 5 wherein said at least one source and at least one drain are laid out in a substantially checkerboard pattern.

8. A semiconductor device comprising:

a. semiconductor substrate;

b. at least one first doped region in said semiconductor substrate forming at least one source;

c. at least one second doped region in said semiconductor substrate forming at least one drain;

d. a first connectivity layer operatively connected to said at least one first doped region;

e. a second connectivity layer operatively connected to said first connectively layer and operatively connected to said at least one second doped region.

9. A semiconductor device of claim 8 wherein said second conductivity layer is operatively connected to said at least one second doped region through said first conductivity layer.

10. A semiconductor device of claim 9 wherein said second conductivity layer is operatively connected to said at least one second doped region through said first conductivity layer and using a portion of said first conductivity layer for such connection.

11. A semiconductor device of claim 8 having a third conductivity layer with at least one first pad and at least one second pad of such layer wherein said at least one first pad is operatively connected to said first connectivity layer and said at least one second pad is operatively connected to said second connectivity layer.

12. A semiconductor device of claim 11 wherein said at least one first pad has at least one first solder bump and said at least one second pad has at least one second solder bump.

13. A semiconductor device of claim 12 wherein said at least one first pad and said at least one second pad are arranged in a substantially checkerboard pattern.

14. A semiconductor device of claim 12 wherein said at least one first pad is interleaved with said at least one second pad.

15. A semiconductor device of claim 8 wherein said at least one source and at least one drain are laid out in a substantially elongated shape and wherein said at least one source are interleaved with said at least one drain.

16. A semiconductor device of claim 8 wherein said at least one source and at least one drain are laid out in a substantially checkerboard pattern.

17. A semiconductor device comprising:

a. semiconductor substrate;

b. at least one first doped region in said semiconductor substrate forming at least one source;

c. at least one second doped region in said semiconductor substrate forming at least one drain;

d. a first connectivity layer having at least one first runner operatively connected to said at least one first doped region and at least one second runner operatively connected to said at least one second doped region;

e. a second connectively layer having at least one first pad operatively connected to said at least one first runner and at least one second pad operatively connected to said at least one second runner.

18. A semiconductor device of claim 17 wherein said at least one first pad has at least one first solder bump and said at least one second pad has at least one second solder bump.

19. A semiconductor device of claim 18 wherein said at least one first pad and said at least one second pad are arranged in a substantially checkerboard pattern.

20. A semiconductor device of claim 18 wherein said at least one first pad is interleaved with said at least one second pad.

21. A semiconductor device of claim 17 wherein said at least one source and at least one drain are laid out in a substantially elongated shape and wherein said at least one source are interleaved with said at least one drain.

22. A semiconductor device of claim 17 wherein said at least one source and at least one drain are laid out in a substantially checkerboard pattern.